IEEE NITK CHAPTER

PROJECT – Designing an ALU

|  |  |
| --- | --- |
|  | **ABSTRACT**  <Briefly explain the abstract> |

# Section 1 – project overview

|  |  |
| --- | --- |
|  | The proposal is divided into two sections namely – Project Overview and Literature Review. The first section will cover the motivation, objectives, methodology, timeline, budget and deliverables of the project. The second section contains the literature review regarding the different phases of the project. |

## The Motivation

No matter the purpose of the processor, ALU forms the most important piece of it. It basically is the heart and soul of an ISA.

## The Opportunity

This project gives an excellent opportunity to learn Digital System Design and implement it in a worthwhile manner.

## The Objective

<Detailed Objective>

## Project Approach

<How will all tasks and workload be divided>

## Project Deliverables

The following are the full list of deliverables which will be achieved through the entire project timeline:

|  |  |
| --- | --- |
| Deliverable | Description |
| Deliverable #1 | Boolean Algebra and Logic gates |
| Deliverable #2 |  |
| Deliverable #3 | Description |
| Deliverable #4 | Description |

<Final Deliverable briefly extra description/conclusion>

## Timeline for Execution

Key project dates are outlined below. Dates are best-guess estimates and are subject to change until a contract is executed.

|  |  |
| --- | --- |
|  | In the Table below, the dates and duration of the project are tentative and subjected to change as it depends on the availability of resources to accomplish some tasks. |

|  |  |  |  |
| --- | --- | --- | --- |
| Description | Start Date | End Date | Duration |
| Project Phase 1 | | | |
| Milestone 1: Learning Boolean Algebra and Logic gates  Description |  |  |  |
| Milestone 2: Combinational and Sequential  Description |  |  |  |
| Project Phase 2 | | | |
| Milestone 3: Implementing basic logic gates on Verilog  Description |  |  |  |
| Milestone 4: Learning ISA  Description |  |  |  |
| Project Phase 3 | | | |
| Milestone 5: Implementing the ALU  Description |  |  |  |
| Milestone 6: Optimizing the ALU  Description |  |  |  |
| Project Phase 4 | | | |
| Milestone 7: Implementing the CU  Description |  |  |  |
| Project Phase 5 | | | |
| Milestone 8: Learning Assembly Code, Register File and Data Memory  Description |  |  |  |
| Project End | | | |

## Budget

|  |  |
| --- | --- |
|  | Disclaimer: The prices listed in the preceding table are an estimate for the services discussed. This summary is not a warranty of final price. Estimates are subject to change if project specifications are changed or costs for outsourced services change before a contract is executed. |

<Brief Introduction to budget division if required>

|  |  |
| --- | --- |
| Name of Item | Estimated Price |
| Division 1 | |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
| **Total:** |  |
| Division 2 | |
|  |  |
|  |  |
| **Total:** |  |
| Other | |
|  |  |
| Estimated Total |  |

## References

<References links>

# SECTION 2 – LITERATURE REVIEW

## Introduction